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15:26:45          OCA PAD AMENDMENT - PROJECT HEADER INFORMATION          04/05/94

                                                                            Active
Project #: E-24-687            Cost share #:                    Rev #: 1
Center # : 10/24-6-R7688-0A0   Center shr #:                    OCA file #:
                                                                Work type : RES
Contract#: DDM-9215467                   Mod #: AMENDMENT 001   Document  : GRANT
Prime    #:                                                     Contract entity: GTRC

Subprojects ? : N                                               CFDA: 47.041
Main project #:                                                 PE #: NA


Project unit:              ISYE          Unit code: 02.010.124
Project director(s):
    AMMONS J C             ISYE          (404)894-2364
    TOVEY C A              ISYE          (404)-
    MCGINNIS L F           ISYE          (404)894-2363


Sponsor/division names: NATL SCIENCE FOUNDATION         / GENERAL
Sponsor/division codes: 107                             / 000


Award period:     921201    to    950531  (performance)    960831  (reports)

Sponsor amount          New this change              Total to date
     Contract value                0.00                 300,000.00
     Funded                  100,000.00                 200,000.00
Cost sharing amount                                           0.00

Does subcontracting plan apply ?: N

Title: PROCESS OPTIMIZATION FOR CIRCUIT CARD ASSEMBLY


                              PROJECT ADMINISTRATION DATA

OCA contact: Jacquelyn L. Tyndall      894-4820

 Sponsor technical contact                Sponsor issuing office

 F. HANK GRANT                            MARTIN V. GEARY
 (202)357-5167                            (202)357-9602

 NATIONAL SCIENCE FOUNDATION              NATIONAL SCIENCE FOUNDATION
 1800 G STREET, NW                        1800 G STREET, NW
 WASHINGTON, DC 20550                     WASHINGTON, DC 20550


Security class (U,C,S,TS) : U             ONR resident rep. is ACO (Y/N): N
Defense priority rating   :   N/A         NSF supplemental sheet
Equipment title vests with:    Sponsor         GIT X

Administrative comments -
  AMENDMENT NO. 1 ADDS $100,000 TO PROJECT FOR YEAR 2.
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CA8120

Georgia Institute of Technology
Office of Contract Administration
PROJECT CLOSEOUT - NOTICE

Page: 1
31-JUL-1997 08:21

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Closeout Notice Date 30-JUL-1997 (11)

Project Number E-24-687

Doch Id 44938

Center Number 10/24-6-R7688-0A0

Project Director AMMONS, JANE

Project Unit ISYE

Sponsor NATL SCIENCE FOUNDATION/GENERAL

Division Id 3393

Contract Number DDM-9215467

Contract Entity GTRC

Prime Contract Number

Title PROCESS OPTIMIZATION FOR CIRCUIT CARD ASSEMBLY

Effective Completion Date 31-MAY-1997 (Performance) 31-AUG-1997 (Reports)

Closeout Action:	Y/N	Date Submitted
Final Invoice or Copy of Final Invoice	N	
Final Report of Inventions and/or Subcontracts	N	
Government Property Inventory and Related Certificate	N	
Classified Material Certificate	N	
Release and Assignment	N	
Other	N	

Comments
CREATE DATE IS INCORRECT. SHOULD BE 7-30-97.

Distribution Required:	
Project Director/Principal Investigator	Y
Research Administrative Network	Y
Accounting	Y
Research Security Department	N
Reports Coordinator	Y
Research Property Team	Y
Supply Services Department	Y
Georgia Tech Research Corporation	Y
Project File	Y

E-25-687
#1

5R635

Process Optimization for Circuit Card Assembly

Award No. DDM-9215467

PART II - SUMMARY OF COMPLETED PROJECT (for public use)

The objective of this research is to establish the methodological foundation for computer aided process planning of printed circuit card assemblies. Our focus includes the development of comprehensive models for representing both the assemblies and the technologies of assembly, developing models of the assembly process organization and operation, developing models and necessary methods for generating process plans, and demonstrating methodological developments through case studies in industry.

Algorithms are needed to solve several problems, ranging from single board single machine process optimization to forming groups of boards to run on multiple production lines. For all of these problems, each individual case of the problem will be different, due to both mechanical and procedural variations at the site. The research task for this three year project is to find *generic models* to each problem so that useful generic solution methods can be derived. The idea is that one would need to add site-specific elements for any actual implementation, but it should be easier to build and evaluate a solution based on our generic models and heuristics.

Another major research challenge is to design *heuristics* that are general enough to operate on generic solution forms, yet provide solutions of good quality at reasonable computational expense. The research is proceeding along three major avenues: objective function based optimization, approximate decomposition into classical combinatorial optimization problems, and mathematical programming.

PART III - TECHNICAL INFORMATION (for program management use)

J.C. Ammons, M. Carlyle, L. Cranmer, G.W. DePuy, K.P. Ellis, L.F. McGinnis, C.A. Tovey and H. Xu, "Component Allocation to Balance Workload in Printed Circuit Card Assembly Systems," submitted to *IIE Transactions*, 1993.

Baxter, Lawrence A., Sarid Baxter,, and Craig Tovey, "A Simple Heuristic to Minimize Makespan on Parallel Processors with Unequal Capacities," submitted to *Operations Research* as a Technical Note, 1993.

L.F. McGinnis, J.C. Ammons, C.A. Tovey, "Circuit Card Assembly Process Planning," *Proceedings of the ASME Winter Annual Meeting*, New Orleans, LA, November 20-December 1, 1993.

E-24-687
2

To NSF Program: Production Systems

APPENDIX VIII

Annual NSF Grant Progress Report

PI Name: Jane C. Ammons

NSF Award Number: DDM-9215467

PI Institution: Georgia Tech Institute of Technology

PI Address:
School of Industrial and
Systems Engineering
Atlanta, GA 30332-0205

Date: August 29, 1994

I certify that to the best of my knowledge (1) the statements herein (excluding scientific hypotheses and scientific opinions) are true and complete, and (2) the text and graphics in this report as well as any accompanying publications or other documents, unless otherwise indicated, are the original work of the signatories or individuals working under their supervision. I understand that the willful provision of false information or concealing a material fact in this report or any other communication submitted to NSF is a criminal offense (U.S.Code, Title 18, Section 1001.)

Signature: ______________________________

Please include the following information:

1. A brief summary of overall progress, including results obtained to date, their relationship to the general goals of the award and their significance to science;
2. an indication of any current problems or favorable or unusual developments;
3. a brief summary of work to be performed during the next year of support if changed from the original proposal; and
4. any other information pertinent to the type of project supported by NSF or as specified by the terms and conditions of the grant.

If applicable, please attach a copy of any updated human subject or animal subject certification.
[Attach additonal sheets as necessary.]

Process Optimization for Circuit Card Assembly   Award No. DDM-9215467

1. BRIEF SUMMARY OF OVERALL PROGRESS

The objective of this research is to establish the methodological foundation for computer aided process planning of printed circuit card assemblies. Our focus includes the development of comprehensive models for representing both the assemblies and the technologies of assembly, developing models of the assembly process organization and operation, developing models and necessary methods for generating process plans, and demonstrating methodological developments through case studies in industry.

Algorithms are needed to solve several problems, ranging from single board single machine process optimization to forming groups of boards to run on multiple production lines. For all of these problems, each individual case of the problem will be different, due to both mechanical and procedural variations at the site. The research task for this three year project is to find *generic models* to each problem so that useful generic solution methods can be derived. The idea is that one would need to add site-specific elements for any actual implementation, but it should be easier to build and evaluate a solution based on our generic models and heuristics.

This project has been funded for two years. During this time we have developed models and solution approaches to 1) optimize machine feeder setup and placement sequencing for one board type for specific placement equipment models, and 2) allocate component types to machine in order to balance the workload among machines. The algorithms have been implemented and models verified and validated using case studies from several industry partners. This past year our efforts have included 1) algorithmic development and implementation of process optimization algorithms for the Universal 4780 placement machine, 2) extension of initial results for component allocation to better incorporate machine operation considerations, and 3) investigation of interrelated problems and associated models for decisions which are at higher levels in the setup management hierarchy.

Thus far our research has broken new ground with comprehensive models and solution approaches which fit a variety of electronic production environments. Case study validation in industry had indicated significant production efficiencies, with some companies reporting savings in the range of several million dollars per year. In addition, significant savings of engineering effort have been confirmed. Specific results have been reported as follows.

Refereed Publications

J.C. Ammons, M. Carlyle, L. Cranmer, G.W. DePuy, K.P. Ellis, L.F. McGinnis, C.A. Tovey, and H. Xu, "Component Allocation to Balance Workload in Printed Circuit Card Assembly Systems," submitted to *IIE Transactions*, 1993.

Baxter, Lawrence A., Sarid Baxter,, and Craig Tovey, "A Simple Heuristic to Minimize Makespan on Parallel Processors with Unequal Capacities," submitted to *Operations Research* as a Technical Note, 1993.

Conference Proceedings

L.F. McGinnis, J.C. Ammons, and C.A. Tovey, "Circuit Card Assembly Process Planning," *Proceedings ASME Winter Annual Meeting*, New Orleans, Louisiana, November 29 - December 1, 1993.

J.C. Ammons, G.W. DePuy, K.P. Ellis, M. Fisher, L.F. McGinnis, and C.A. Tovey, "Process Optimization for Circuit Card Assembly," *Proceedings of the 1994 NSF Grantees Conference on Design and Manufacturing Systems Research*, Cambridge, Massachusetts, January 5-7, 1994.

Presentations

"Setup Management in Electronic Assembly Systems"
1994 Graduate Symposium: Technology Transfer - Real Research for a Real World Atlanta, Georgia, February 17, 1994.

"Component Allocation to Balance Workloads in Electronic Assembly"
1994 Graduate Symposium: Technology Transfer - Real Research for a Real World Atlanta, Georgia, February 17, 1994.

"Process Optimization for Printed Circuit Card Assembly"
Manufacturing Engineering Seminar
Auburn Univerisity, Alabama, April 12, 1994.

"New Results on the Old K-Opt Algorithm for the Traveling Salesman Problem," TIMS/ORSA Conference
Boston, Massachusetts, April 24-27, 1994.

"Electronic Assembly Research"
Industrial Engineering Research Conference
Atlanta, Georgia, May 18-19, 1994.

"Process Optimization for Printed Circuit Card Assembly"
Second Annual Border Conference on Manufacturing and the Environment
El Paso, Texas, May 24-25, 1994.

2. FAVORABLE DEVELOPMENTS

The National Science Foundation grant has been leveraged with funding from the Georgia Tech Manufacturing Research Center, a consortium of industry contributors which include Ford Electronics, Motorola, AT&T, and MICOM. The industry interaction provides an excellent environment for problem definition, model formulation, and case study development. An algorithmic implementation for single board optimization of a specific type of placement equipment has been delivered to engineers within each of these companies.

3. CHANGES IN PLAN FOR WORK IN UPCOMING YEAR

No major changes are planned. The focus of our work will be driven by the original research plan submitted in our proposal to the NSF, the specific production interests of the companies listed above, and the reality that during the upcoming year two of the students will be finishing their dissertations on component allocation/workload balance and on setup management decision strategies.

4. OTHER PERTINENT INFORMATION

Mark Fisher, one of the students employed by this project, received his Masters Science of Computer Science in 1994 and is now working in industry. The project now employs two femal Ph.D. students in Industrial Engineering.

E-24-681 #3

OMB Number 345-0058

NATIONAL SCIENCE FOUNDATION
4201 Wilson Blvd.,
Arlington, VA 22230

BULK RATE
POSTAGE & FEES PAID
National Science Foundation
Permit No. G-69

PI/PD Name and Address

Jane C. Ammons
School of Industrial and Systems
[redacted]
Engineering
Atlanta GA 30332

NATIONAL SCIENCE FOUNDATION FINAL PROJECT REPORT

PART I - PROJECT IDENTIFICATION INFORMATION

1. Program Official/Org. Georgia-Ann Klutke - DMI

2. Program Name OPERATIONS RESEARCH & PRODUCTION SYSTEMS

3. Award Dates (MM/YY) From: 12/92 To: 05/97

4. Institution and Address

[redacted]
Administration Building
Atlanta GA 30332

5. Award Number 9215467

6. Project Title

Process Optimization for Circuit Card Assembly

** You are encouraged to submit your Final Project Report electronically **
** through the NSF FastLane home page (www.fastlane.nsf.gov). **

This Packet Contains
NSF Form 98A
And 1 Return Envelope

NSF Grant Conditions (Article 17, GC-1, and Article 8, FDP-II) require submission of a Final Project Report (NSF Form 98A) to the NSF Program Officer no later than 90 days after the expiration of the award. Final Project Reports for expired awards must be received before new awards can be made (NSF Grants Policy Manual Section 340).

Below, or on a separate page attached to this form, provide a summary of the completed projects and technical information. Be sure to include your name and award number on each separate page. See below for more instructions.

PART II - SUMMARY OF COMPLETED PROJECT (for public use)

The summary (about 200 words) must be self-contained and intelligible to a scientifically or technically literate reader. Without restating the project title, it should begin with a topic sentence stating the project's major thesis. The summary should include, if pertinent to the project being described, the following items:

- The primary objectives and scope of the project
- The techniques or approaches used only to the degree necessary for comprehension
- The findings and implications stated as concisely and informatively as possible

The thrust of this project was to establish a methodological foundation for computer aided process planning for printed circuit card assembly. The goal was to develop an approach and the necessary methodologies and tools to allow circuit card assembly manufacturers to determine the optimal strategy for circuit card assembly, and to rapidly generate optimal or near-optimal plans. The objective was to maximize total production rate over a desired product mix. The constraints were the equipment capabilities, including material handling, the products' bills of materials, component, technologies, and the production plan (quantities and lot sizes required) for some planning horizon. Our research challenge was to find generic qualities or characteristics about each problem so that we could derive useful generic solution methods. The idea is that one would need to add site-specific elements for any actual implementation, but it should be easier to build and evaluate a specific solution based on our generic models and heuristics.

Two types of results were obtained from the research. First, models and algorithms were developed for the process optimization for a range of assembly equipment types. These algorithms were demonstrated using case study data from actual circuit card assembly operations. Ultimately, these algorithms should provide the basis for automated or semi-automated process planning tools. Such tools enable process planners to create higher quality process plans, with much shorter lead times than is currently possible. The potential benefit to manufacturing is faster response to changing requirements and continuous improvement of the assembly process.

Second, given a particular setup management strategy, models and algorithms were developed for optimizing the assignment of components among assembly equipment and the grouping and sequencing of card types within the assembly system material flow. In addition, the research explored methods for comparing alternative setup management strategies and for selecting the best strategy for a given situation.

PART III - TECHNICAL INFORMATION (for program management use)

List references to publications resulting from this award and briefly describe primary data, samples, physical collections, inventions, software, etc., created or gathered in the course of the research and, if appropriate, how they are being made available to the research community. Provide the NSF Invention Disclosure number for any invention.

Ammons, J.C., M. Carlyle, G.W. DePuy, K.P. Ellis, L.F. McGinnis, C. A. Tovey, and H. Xu, "Computer Aided Process Planning in Printed Circuit Card Assembly," *Proceedings of the International Electronics Manufacturing Technology Symposium*, Baltimore, Maryland, September 28-30, 1992.

McGinnis, L.F., J.C. Ammons, M. Carlyle, L. Cranmer, G.W. DePuy, K.P. Ellis, C. A. Tovey, and H. Xu, "Automated Process Planning for Printed Circuit Card Assembly," *IIE Transactions on Scheduling and Logistics*, Vol. 24, No. 4, September 1992, pp.18-30.

Ammons, J.C., M. Carlyle, G.W. DePuy, K.P. Ellis, L.F. McGinnis, C. A. Tovey, and H. Xu, "Productivity Improvements in SMD Placement Through CAPP," *Proceedings of the International Society of Hybrid Microelectronics Conference*, San Francisco, California, October 19-21, 1992.

Ammons, J.C., M. Carlyle, G.W. DePuy, K.P. Ellis, L.G. McGinnis, C.A. Tovey, and H. Xu, "Computer Aided Process Planning in Printed Circuit Card Assembly," *IEEE-CHMT Transactions*, Vol. 16, No. 4, June, 1993.

Ammons, J.C., M. Carlyle, G.W. DePuy, K.P. Ellis, M. Fisher, L.F. McGinnis, C.A. Tovey, and H. Xu, "Process Optimization for Circuit Card Assembly," *Proceedings of the 1993 NSF Design and Manufacturing Systems Conference*, Charlotte, NC, January 6-8, 1993.

Ammons, J.C., G.W. DePuy, K.P. Ellis, M. Fisher, L.F. McGinnis, and C.A. Tovey, "Process Optimization for Circuit Card Assembly," *Proceedings of the 1994 NSF Design and Manufacturing Systems Conference, Boston, MA*, January 5-7, 1994.

DePuy, Gail W., "Component Allocation to Balance Workload in Printed Circuit Card Assembly," Ph.D. Dissertation in the School of Industrial and Systems Engineering at The Georgia Institute of Technology, Atlanta, GA, August 1995.

Ammons, J.C., G.W. DePuy, K.P. Ellis, L.F. McGinnis, and C.A. Tovey, "Process Optimization for Circuit Card Assembly," *Proceedings of the 1995 NSF Design, Manufacturing, and Industrial Innovation Conference*, San Diego, January 3-5, 1995.

Baxter, L., F. Harche, and C. Tovey, "A simple heuristic to minimize makespan on parallel processors with unequal capacities," *International Journal of Operations and Quantitative Management*, Vol. 1, 1995.

Ammons, J.C., G.W. DePuy, K.P. Ellis, L.F. McGinnis, and C.A. Tovey, "Process Optimization for Circuit Card Assembly," *Proceedings of the 1996 NSF Design, Manufacturing, and Industrial Innovation Conference*, January 3-5, 1996.

Ellis, Kimberly P., "Analysis of Set-up Strategies in Electronic Assembly Systems," Ph.D. Dissertation in the School of Industrial and Systems Engineering at The Georgia Institute of Technology, Atlanta, GA, June 1996.

Ammons, J.C., K.P. Ellis, G.W. DePuy, L.F. McGinnis, and C.A. Tovey, "Process Optimization for Electronic Assembly Systems--Industrial Case Studies, " *Proceedings of the 5th Industrial Engineering Research Conference*, Minneapolis, Minnesota, May 18-20, 1996.

Ammons, J.C., M. Carlyle, L. Cranmer, G.W. DePuy, K.P. Ellis, L.G. McGinnis, C.A. Tovey, and H. Xu, "Component Allocation to Balance Workload in Printed Circuit Card Assembly Systems," *IIE Transactions*, Vol. 29, pp. 265-275, 1997.

DePuy, G., J.C. Ammons, and L.F. McGinnis, "Formulation of a General Component Allocation Model for Printed Circuit Card Assembly Systems," *Proceedings of the 6th Industrial Engineering Research Conference*, Miami, FL, May, 1997.

DePuy, G.W., M.W.P. Savelsbergh, J.C. Ammons, and L.F. McGinnis, "An Integer Programming Heuristic for Component Allocation in Printed Circuit Card Assembly Systems," working paper, revised June 1997.

Ellis, K.P., L.F. McGinnis, and J.C. Ammons, "Setup Management Issues in Printed Circuit Card Assembly Systems, " *Proceedings of the Factory Automation International Manufacturing Conference*, Manchester, England, October, 1997.

Chandra, B., H. Karloff, and C. Tovey, "New results on the old k-opt algorithm for the traveling salesman problem," forthcoming in *SIAM Journal on Computing*.

I certify to the best of my knowledge (1) the statements herein (excluding scientific hypotheses and scientific opinion) are true and complete, and (2) the text and graphics in this report as well as any accompanying publications or other documents, unless otherwise indicated, are the original work of the signatories or of individuals working under their supervision. I understand that willfully making a false statement or concealing a material fact in this report or any other communication submitted to NSF is a criminal offense (U.S. Code, Title 18, Section 1001).

	June 11, 1997
Principal Investigator/Project Director Signature	Date

IMPORTANT:
MAILING INSTRUCTIONS
Return this *entire* packet plus all attachments in the envelope attached to the back of this form. Please copy the information from Part 1, Block I to the *Attention block* on the envelope.

NSF Form 98A (Rev. 7/95)

PART IV - FINAL PROJECT REPORT – SUMMARY DATA ON PROJECT PERSONNEL

(To be submitted to cognizant Program Officer upon completion of project)

The data requested below are important for the development of a statistical profile on the personnel supported by Federal grants. The information on this part is solicited in response to public Law 99-383 and 42 USC 1885C. All information provided will be treated as confidential and will be safeguarded in accordance with the provisions of the Privacy Act of 1974. You should submit a single copy of this part with each final project report. However, submission of the requested information is not mandatory and is not a precondition of future award(s). Check the "Decline to Provide Information" box below if you do not wish to provide the information.

Please enter the numbers of individuals supported under this grant.
Do not enter information for individuals working less than 40 hours in any calendar year.

	Senior Staff		Post Doctorals		Graduate Students		Under-Graduates		Other Participants[1]	
	Male	Fem.	Male	Fem.	Male	Fem.	Male	Fem.	Male	Fem.
A. Total, U.S. Citizens	2	1	0	0	1	3	1	0		
B. Total, Permanent Residents										
U.S. Citizens or Permanent Residents:[2] American Indian or Alaskan Native....										
Asian..										
Black, Not of Hispanic Origin............										
Hispanic...										
Pacific Islander................................										
White, Not of Hispanic Origin............	2	1	0	0	1	3	1	0		
C. Total, Other Non-U.S. Citizens										
Specify Country 1. P.R. China						1				
2.										
3.										
D. Total, All participants (A + B + C)	2	1	0	0	1	4	1	0		
Disabled[3]										

☐ Decline to Provide Information: Check box if you do not wish to provide this information (you are still required to return this page along with parts I-III).

[1] Category includes, for example, college and precollege teachers, conference and workshop participants.

[2] Use the category that best describes the ethnic/racial status to all U.S. Citizens and Non-citizens with Permanent Residency. *(If more than one category applies, use the one category that most closely reflects the person's recognition in the community.)*

[3] A person having a physical or mental impairment that substantially limits one or more major life activities; who has a record of such impairment; or who is regarded as having such impairment. (*Disabled individuals also should be counted under the appropriate ethnic/racial group unless they are classified as "Other Non-U.S. Citizens."*)

AMERICAN INDIAN OR ALASKAN NATIVE: A person having origins in any of the original peoples of North America and who maintains cultural identification through tribal affiliation or community recognition.

ASIAN: A person having origins in any of the original peoples of East Asia, Southeast Asia or the Indian subcontinent. This area includes, for example, China, India, Indonesia, Japan, Korea and Vietnam.

BLACK, NOT OF HISPANIC ORIGIN: A person having origins in any of the black racial groups of Africa.

HISPANIC: A person of Mexican, Puerto Rican, Cuban, Central or South American or other Spanish culture or origin, regardless of race.

PACIFIC ISLANDER: A person having origins in any of the original peoples of Hawaii, the U.S. Pacific territories of Guam, American Samoa, and the Northern Marinas; the U.S. Trust Territory of Palau; the islands of Micronesia and Melanesia; or the Philippines.

WHITE, NOT OF HISPANIC ORIGIN: A person having origins in any of the original peoples of Europe, North Africa, or the Middle East.

NSF Form 98A (Rev. 7/95)